AMENDMENTS TO THE CLAIMS

9. (currently amended) A memory device comprising:

a gate stack pair with a space between them defining a contact opening;

a vertical oxide spacer adjacent to each gate stack of said gate stack pair; and

a respective continuous nitride layer overlaying each said vertical oxide spacer and each said gate stack, neither of said continuous nitride layers extending to overlay ~~cover~~ said contact opening between said gate stack pair.

10. (original) The memory device of claim 9, wherein said gate stack comprises a floating gate and a control gate.

11. (original) The memory device of claim 9, wherein said vertical oxide spacer is between about 50Å and about 300Å in thickness.

12. (original) The memory device of claim 9, wherein said vertical oxide spacer is about 100Å and about 200Å in thickness.

13. (original) The memory device of claim 9, wherein said nitride layer has a thickness equal to about one half the width of said vertical oxide spacer.